

## REMARKS

### **Status of Claims:**

By way of the instant amendment, claims 8-11 have been added. Thus, claims 1-11 remain for examination.

### **Drawing Corrections:**

Submitted herewith are replacement sheets of Figs. 2, 3, 4, 6 and 7. These replacement sheets correct the spelling errors noted in paragraph 4 of the outstanding Office Action. In addition, "SHIFTREGISTER" in Fig's. 2 and 4 has been changed to --SHIFT REGISTER--.

### **Claim Objections:**

The objections to claims 1, 3 and 5 as stated in paragraph 5 of the outstanding Office Action have been corrected by way of the instant amendment.

With regard to claims 4 and 5, applicant has amended these claims to recite that only the second and third selectors are switched at each time interval of  $T/n$  to be consistent with the written description and Fig. 6.

### **Rejections Under Section 112:**

Claims 4-7 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. The Examiner questions the use of the terms "two parts" and "m parts".

In reply, applicant has amended claims 4-7 to more clearly state applicant's invention. For example, in claim 4, it is stated that the first, second and third selectors and the first and second multipliers are doubled in quantity to form two circuits, each circuit having one of two first selectors, one of two second selectors, one of two third selectors, one of two first multipliers and one of two second multipliers. Each of the two circuits handles only half of the delayed data. Similar changes have been made to the remaining claims 4-7. It is thus

**Prior Art Rejections:**

Claim 1 stands rejected under 35 U.S.C. § 103 as unpatentable over Wittig. Claims 2 and 3 stand rejected under 35 U.S.C. § 103 as unpatentable over applicant's admitted prior art in view of Wittig.

The Examiner's rejections are respectfully traversed.

Applicant has now amended independent claims 1 and 3 in order to more clearly define applicant's invention over the applied prior art. In particular, claim 1 now recites the variable gain digital filter operating on input data and providing delayed input data, including power control bits, as a portion of the delayed input data. The digital filter further provides non-power control bits as another portion of the delayed input data. The digital filter has a construction in which a gain regulation circuit is incorporated inside the digital filter. The gain regulator circuit comprises a first selector for selecting a first gain signal corresponding to the power control bits and a second gain signal corresponding to the non-power control bits. The regulator circuit also includes a first multiplier for directly multiplying some coefficient sequences with the first gain signal and other coefficient sequences with the second gain signal. The first and second gain signals are output from the first selector. The recitation of the first and second gain signals in combination with the other limitations set forth in claim 1 are not disclosed in applicant's admitted prior art nor in the Wittig disclosure.

Claim 3 is more narrowly drafted than claim 1 but likewise recites the power control bits as part of the delayed data and the first and second gain signals. As such, it is submitted that applicant's independent claims 1 and 3 clearly define over the prior art and are patentable thereover. Dependent claims 2 and 4-7 are likewise deemed patentable at least by virtue of their dependency on independent claims 1 and 3.

Applicants note that no prior art rejections have been applied to claims 4-7. Newly submitted claims 8-11 correspond to the independent versions of claims 4-7, respectively. In drafting these new independent claims 8-11, applicant has been mindful of the § 112 rejections applied to the prior claims, including the base claim 3. It is submitted that

claims 8-11 fully comply with the provisions of 35 U.S.C. § 112 and are furthermore patentable over the prior art.

**Conclusions:**

In view of the amendments made hereto and the remarks set forth above, it is submitted that the application is now in condition for allowance and an early indication of same is earnestly solicited.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

Date 12-9-04

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